

Surajit Das

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EDUCATION

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| Ph.D., Indian Institute of Technology Guwahati, <i>Department of Computer Science and Engineering, Formal Verification, Deadlock Detection and Deadlock Free Routing algorithm in Network-on-Chip</i> | <i>July 2014– Dec 2021</i> |
| M.Tech. National Institute of Technology Jaipur, <i>Computer Engineering</i> | <i>July 2012 - June 2014</i> |
| B.E., Jorhat Engineering College, Jorhat, <i>Computer Science and Engineering</i> | <i>July 2000 - June 2004</i> |
| Class: 12, Cotton College, Guwahati | <i>July 1997–June 1999</i> |
| Class: 10, Vidyabhawan Nityananda High School, Assam | <i>Jan 1991 – May 1997</i> |

WORK EXPERIENCE

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| IIT Guwahati Technology Innovation Development Foundation (IITG TIDF), India <i>Faculty Fellow</i> | <i>Dec 2023 – Till Date</i> |
| Intel India Bangalore and IIT Guwahati, India <i>Post Doctoral Research Associate</i> | <i>Oct 2022 – Aug 2023</i> |
| GITAM School of Technology, Bangalore, India <i>Assistant Professor</i> | <i>March 2022 – Sept 2022</i> |
| Wipro Technology, Bangalore, India <i>Project Engineer</i> | <i>Aug 2006 – Oct 2008</i> |

PUBLICATIONS

Journals

- **Surajit Das**, Chandan Karfa and Santosh Biswas. "Formal Modeling of Network-on-Chip Using CFMSM and its Application in Detecting Deadlock", **IEEE Transactions on Very Large Scale Integration Systems (TVLSI)** , vol. 28, no. 4, pp. 1016-1029, April 2020, doi: 10.1109/TVLSI.2019.2959618.
- **Surajit Das** and Chandan Karfa. "Arc Model and DDG: Deadlock Avoidance and Detection in Torus NoC", **IEEE Embedded Systems Letters (ESL)**, September 2021, doi: 10.1109/LES.2021.3113355.
- **Surajit Das**, Chandan Karfa and Santosh Biswas. "Accelerating NoC Verification using a Complete Model and Active Window", **IEEE Access**, Vol. 10, pp. 88985-88999, 2022, Print ISSN: 2169-3536, Online ISSN: 2169-3536, DOI: 10.1109/ACCESS.2022.3199671.

Submitted Paper

- **Surajit Das**, Abhijit Das and Chandan Karfa. "A Formal Technique Towards Developing Deadlock-Free Routing Algorithms in Torus NoC". (Submitted to IEEE TCAD)

Conference Papers

- **Surajit Das**, Chandan Karfa, Arijit Sur, Hetang Patel, Kartheek B., Rahul R., Disha Puri and Anshul Jain, "RTL Simulation Acceleration with Machine Learning Models," *2024 25th International Symposium on Quality Electronic Design (ISQED)*, San Francisco, CA, USA, 2024, pp. 1-7.

- **Surajit Das** and Chandan Karfa, "Deadlock Avoidance in Torus NoC Applying Controlled Move via Wraparound Channels", 10th **Embedded Computing and System Design (ISED)**, vol. 811, pp. 87--99, December 2021.
- **Surajit Das** and Chandan Karfa, "Formal Modeling and Verification of Starvation-Freedom in NoCs", 10th **Embedded Computing and System Design (ISED)**, vol. 811, pp. 101--114, December 2021.
- **Surajit Das**, Chandan Karfa and Santosh Biswas, "xMAS Based Accurate Modeling and Progress Verification of NoCs", **VLSI Design and Test (VDAT)**, vol. 711, pp. 792-804, July 2017.
- **Surajit Das**, Shirshendu Das and H. K. Kapoor, "Tag only storage for capacity optimised last level cache in chip-multiprocessors", 2016 20th International Symposium on **VLSI Design and Test (VDAT)**, 2016, pp. 1-6.

COURSE INSTRUCTOR

Gandhi Institute of Technology, Bangalore

- Computer Organization and Architecture

March-Sept 2022

TEACHING ASSISTANT

NPTEL Courses

- C-Based VLSI Design

July-Sept 2021

- Optimization Technique in Digital VLSI Design

Jan-March 2018

Indian Institute of Technology Guwahati, India

July 2014 – December 2021

- CS101: Introduction to computing lab (C Programming)
- CS221: Digital Logic
- CS201: Data Structure Lab
- CS222: Computer Organization and Architecture
- CS577: C-Based VLSI Design
- CS591: Data Structure and Algorithm

National Institute of Technology Jaipur, India

July 2012 -May 2014

- C Programming Lab
- System Design Lab

WORKSHOP & TRAINING

- Served as a coordinating team member for the "International Workshop on Dam Safety 2024" held at IIT Guwahati from June 27th to 29th, 2024.
- Coordinated as a team member for a certificate program on "Drone and Anti-Drone Technology" for defense personnel, conducted from April 16th to April 25th, 2024, at TIH, IIT Guwahati.
- Actively participated as a team member in coordinating the "4th International Conference on River Corridor Research and Management" held from March 7th to 9th, 2024, at IIT Guwahati.
- Served as a resource person for a TEQIP-III Sponsored Short Term Course on "C-Based VLSI Design: Synthesis, Optimization, and Verification" held at IIT Guwahati from April 1st to 5th, 2019.
- Actively volunteered for a TEQIP-III Sponsored Short Term Course on "C-Based VLSI Design: Synthesis, Optimization, and Verification" held at IIT Guwahati from April 1st to 5th, 2019.
- Participated in a GiAN course on "Modeling and Verification of Cyber-Physical Systems" at IIT Guwahati from January 1st to 5th, 2018.
- Actively volunteered as a member of the organizing committee for the "20th International Symposium on VLSI Design and Test (VDAT 2016)" held at IIT Guwahati from May 24th to 27th, 2016.
- Actively volunteered as a member of the organizing committee for the "Women in Computing, East and North-East (ACMW 2015).

ACHIEVEMENTS

- Received Intel India Fellowship 2022-2023 as a Post-Doctoral Research Associate.
- MHRD/(MoE) Scholarship for Ph.D (2014-2019).
- MHRD/(MoE) Scholarship for M. Tech. (2012-2014).

- Qualified GATE 2012, 2014.
- Qualified GRE (Graduate Record Examination) in July 2009.
- Qualified TOEFL (Test of English as a Foreign Language) in August 2009.
- Received post-matric scholarship from the Secondary Education Board of Assam in 1997.

DOCTORAL THESIS (Under the supervision of Dr. Chandan Karfa and Prof. Santosh Biswas)

Title: *Formal Modeling of Network-on-Chip and its Applications in Starvation and Deadlock Detection and in Developing Deadlock Free Routing Algorithms.*

Objectives: The objective of this thesis is to develop a formal model of NoC considering the NoC component in detail for detection of starvation and deadlock. The thesis developed a formal model based simulation framework for deadlock detection with deadlock scenarios. The deadlock scenarios after deadlock detection are used in formulating deadlock avoidance for Torus. Using the proposed deadlock avoidance approach, the thesis demonstrated deadlock free routing algorithms for Torus NoC without using additional resources. The main contributions are listed below,

- Formal modeling of NoC using Finite State Machine (FSM) and used the model for verification of starvation freedom and successful transfer of packets.
Formal modeling of NoC using Communicating Finite State Machine (CFSM) and develop a simulation framework using
- the CFSM based NoC model. The CFSM based framework is detects confirmed deadlock on a given application for a particular routing algorithm in a given NoC topology.
- Propose an Arc Model for deadlock avoidance in Torus NoC. A directional dependency graph (DDG) is also proposed for the convenient deadlock representation in Torus NoC.
- Deadlock-free routing algorithms for Torus NoC are proposed using the proposed Arc Model and DDG. Our proposed algorithms do not use any additional resources for deadlock avoidance.

POST-DOCTORAL RESEARCH (Under the supervision of Dr. Chandan Karfa and Prof. Arijit Sur)

Title: *Machine Learning based output prediction to accelerate register transfer level (RTL) simulation.*

Objectives: The objective of this research is to reduce register transfer level (RTL) simulation time by replacing an RTL module with a Machine Learning model that has significant accuracy. We have considered different combinational and sequential designs in this work. The input signals and output signal for a given circuit is considered as the data set to train the ML model. If significant accuracy is achieved using the ML model corresponding to an RTL implementation, we generate the trained model in C equivalent to that ML model. This trained model is used for RTL simulation.

References

1. Dr. Chandan Karfa
Associate Professor
Dept. of Computer Science and Engineering,
IIT Guwahati, Assam, India, Pin-781039
Email: ckarfa@iitg.ac.in
2. Prof. Santosh Biswas
Professor
Dept. of Electrical Engineering and Computer Science,
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3. Prof. Arijit Sur
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