Curriculum Vitae

1. Personal Details:

Surajit Das

PhD Student, Computer Science and Engineering,

Indian Institute of Technology Guwahati, www.iitg.ac.in

Assam, India, Pin-781039

Email: d.surajit@iitg.ernet.in

Mobile: +91 8724038638

2. Educational Qualification:

Degree	Name of Institute	Year Of Completion	Percentage/CGPA
Ph.D.	Department Of Computer Science and Engineering, IIT Guwahati.	On Going From July 2014.	
M. Tech. ,Computer Science and Engineering	Malaviya National Institute Of Technology, Jaipur.	2014.	CGPA 7.1 on 10 point scale
B.E. , Computer Science and Engineering	Jorhat Engineering College, Jorhat.	2004	59.29%
Higher Secondary (12^{th} Standard)	Cotton College, Guwahati.	1999	65.80%
High School Leaving Certificate (10^{th} Standard)	Vidyabhawan Nityananda High School, Nityananda	1997	76.4%

3. Research Work:

My research areas of interest are Network On Chip, Formal Verification, Cache Memory and Big Data Analysis. In my PhD research work, I am involved in formal verification of Network On Chip. In this research I have designed a generic router for network on chip under supervision of my research guide. Objective of our work is to verify whether the design of a Network On Chip model satisfies some important properties like deadlock freedom, livelock freedom, starvation

freedom, reachability of a packet etc. I am also interested in research on optimizing cache memory.

4. Publications:

No.	Publication Details
1	Surajit Das, Chandan Karfa and Santosh Biswas, “Formal Modeling of Network-on-Chip using CFSM and Its Application in Detecting Deadlock”, IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, vol. 28, no. 4, pp. 1016-1029, April 2020 .
2	Surajit Das and Chandan Karfa. “Arc Model and DDG: Deadlock Avoidance and Detection in Torus NoC”, IEEE Embedded Systems Letters (ESL). (Minor revision: Revised version submitted)
3	Surajit Das and Chandan Karfa, “Deadlock Avoidance in Torus NoC Applying Controlled Move via Wraparound Channels", Embedded Computing and System Design (ISED), 2021. (Accepted)
4	Surajit Das and Chandan Karfa, “Formal Modeling and Verification of Starvation Freedom in NoCs", Embedded Computing and System Design (ISED), 2021. (Accepted)
5	Surajit Das, Chandan Karfa and Santosh Biswas, “xmas based accurate modeling and progress verification of nocs”, In VDAT 2017, pages 792–804.
6	S. Das, S. Das and H. K. Kapoor, "Tag only storage for capacity optimised last level cache in chip multiprocessors," 2016 20th International Symposium on VLSI Design and Test (VDAT), 2016, pp. 1-6, doi: 10.1109/ISVDAT.2016.8064886
7	“Big Data Analysis Issues And Evolution Of Hadoop” S. Das, D. Gopalani, *IJPRET, 2014; Volume 2 (8): 152-161*

6. References:

i.

Dr. Chandan Karfa

Dept. of Computer Science and Engineering,

IIT Guwahati, Assam, India, Pin-781039

Email: ckarfa@iitg.ernet.in

ii.

Dr. Santosh Biswas

Dept. of Computer Science and Engineering,

IIT Guwahati, Assam, India, Pin-781039

Email: santosh_biswas@iitg.ernet.in

iii.

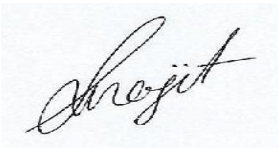
Dr. Dinesh Gopalani

Dept. of Computer Engineering,

Malaviya National Institute Of Technology, Jaipur, Rajasthan, India, Pin-302017

Email: dgopalani.cse@mnit.ac.in

I, hereby, solemnly declare that all the statements made in the above are true and correct to the best of my knowledge and belief.



Surajit Das

Date: 6 August 2021

Place: IIT Guwahati, Assam, India